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S/N 09/945,500PATENTIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes

Examiner: Ly Pham

Serial No.: 09/945,500

Group Art Unit: 2818

Filed: August 30, 2001

Docket: 1303.029US1

Title: PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH
LOW TUNNEL BARRIER INTERPOLY INSULATORSPETITION TO RETURN FORM PTO-1449sCommissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant encloses a copies of the 1449 forms that were submitted with the Information Disclosure Statements filed on July 26, 2002; March 24, 2003; and March 11, 2004. Applicant requests that the examiner initial the 1449 forms and return them with the next communication.

The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date

9/09/04

By

Timothy B Clise
Reg. No. 40,957

I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

Amy J. Moriarty

Date of Transmission

COPY

In re Patent Application of: Leonard Forbes
Title: PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH
LOW TUNNEL BARRIER INTERPOLY INSULATORS
Serial No.: 09/945,500

Filing Date: August 30, 2001
Receipt is hereby acknowledged for the following in the United States Patent and
Trademark Office:

CONTENTS: an Information Disclosure Statement (1 pg.), Form 1449 (2 pgs.), and
copies of 33 cited references; A Communication Concerning Co-Pending Applications (2
pgs.); a Return Postcard and TRANSMITTAL SHEET.

Mailed: July 20, 2002
EJB/gmu

Docket No.: 1303.029US1
Due Date: N/A

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Applicant: Leonard Forbes

Title: PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER
INTERPOLY INSULATORS

Docket No.: 1303.029US1

Serial No.: 09/945,500

Filed: August 30, 2001

Due Date: N/A

Examiner:

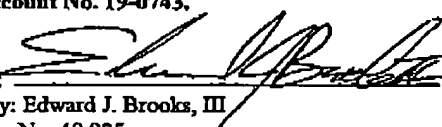

Group Art Unit: 2818

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ An Information Disclosure Statement (1 pg.), Form 1449 (2 pgs.), and copies of 33 cited references.
- ☒ A Communication Concerning Co-Pending Applications (2 pgs.).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)By: 
Atty: Edward J. Brooks, III
Reg. No. 40,925CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 10 day of July, 2002.Name Gina M. UphusSignature 

Customer Number 21186

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

(GENERAL)

JUL 09 2004

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SCHWEGMAN ■ LUNDBERG ■ WOESSNER ■ KLUTH

PATENT, TRADEMARK & COPYRIGHT ATTORNEYS

P.O. Box 2938

Minneapolis, MN 55402

Telephone (612) 373-6900

Facsimile (612) 339-3061

July 9, 2004

Time: 4:45 pm
(Minneapolis, Minn.)TO: Commissioner for Patents
Attn: Ly D. Pham
Patent Examining Corps
Facsimile Center
P.O. Box 1450
Alexandria, VA 22313-1450FROM: Timothy B. CliseOUR REF: 1303.029US1TELEPHONE: 571-272-1793FAX NUMBER 703-872-9306* Please deliver to Examiner Ly D. Pham in Art Unit 2818. *

Document(s) Transmitted: Petition to Return Form PTO-1449s (1 pg.), A copy of Information Disclosure Statement filed on July 26, 2002 (7 pages), A copy of Information Disclosure Statement filed on March 24, 2003 (5 pages), A copy of Information Disclosure Statement filed on March 11, 2004 (5 pages).

Total pages of this transmission, including cover letter: 19 pgs.

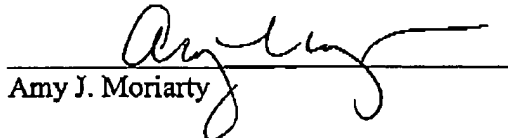
If you do NOT receive all of the pages described above, please telephone us at 612-373-6900 or fax us at 612-339-3061.

In re. Patent Application of: Leonard ForbesExaminer: Ly D. PhamSerial No.: 09/945,500Group Art Unit: 2818Filed: August 30, 2001Docket No.: 1303.029US1Title: PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

Please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

By: Name: Timothy B. CliseReg. No.: _____ Reg. No. 40,957

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Amy J. MoriartyJuly 9, 2004
Date of Transmission

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S/N 09/945,500PATENTIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes Examiner:
Serial No.: 09/945,500 Group Art Unit: 2818
Filed: August 30, 2001 Docket: 1303.029US1
Title: PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH
LOW TUNNEL BARRIER INTERPOLY INSULATORS

COMMUNICATION CONCERNING CO-PENDING APPLICATION(S)

Commissioner for Patents
Washington, D.C. 20231

Applicant would like to bring to the Examiner's attention the following related co-pending application(s) in the above-identified patent application:

| <u>Serial No.</u> | <u>Filing Date</u> | <u>Attorney Docket</u> | <u>Title</u> |
|-------------------|--------------------|------------------------|--|
| 09/256,643 | 02/23/1999 | 00303.324US2 | TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE |
| 09/652,420 | 08/31/2000 | 00303.324US3 | TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE |
| 09/691,004 | 10/18/2000 | 00303.324US4 | TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE |
| 08/903,453 | 07/29/1997 | 00303.378US1 | CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS |
| 09/258,467 | 02/26/1999 | 00303.378US2 | CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS |
| 09/650,553 | 08/30/2000 | 00303.378US3 | CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS |
| 09/669,281 | 09/26/2000 | 00303.405US3 | PROGRAMMABLE MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS |

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COMMUNICATION CONCERNING CO-PENDING APPLICATIONS

Serial Number: 09/945,500

Filing Date: August 30, 2001

Title: PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORSPage 2
Dkt 1303.029US1

| | | | |
|------------|------------|--------------|--|
| 09/780,169 | 02/09/2001 | 01303.003US1 | FLASH MEMORY WITH ULTRATHIN VERTICAL BODY TRANSISTORS |
| 10/152,649 | 02/09/2001 | 01303.003US2 | FLASH MEMORY WITH ULTRATHIN VERTICAL BODY TRANSISTORS |
| 09/945,507 | 08/30/2001 | 01303.014US1 | FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS |

Respectfully submitted,

LEONARD FORBES

By Applicant's Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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Date

7/19/2002

By

Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 23 day of July, 2002.

Gina M. Uphus

Name

Signature

